AC COUPLING SYSTEM FOR WIDE BAND DIGITAL DATA WITH DYNAMIC AC LOAD

INVENTORS

GEORGE W. BROWN AND
THOMAS S. WONG

FIELD OF THE INVENTION

[0001] This invention relates to wide-band, broad spectrum, data communications and more particularly to an interface system for coupling a fixed impedance with a wide-band receiver operating at multiple data rates.

BACKGROUND OF THE INVENTION

[0002] Conventional communications systems typically require an interface system to couple a signal from an output device with low characteristic output impedance (e.g., about 8 to about 500 ohms) to a receiver while producing minimal signal distortion. The low impedance output may be the output of another device, such as a gigabit interface converter (GBIC), or the output of a fixed impedance transmission line, or a serializer/deserializer (SERDES), or the like. Data signals in digital communication systems are typically square waves having at least two voltage levels (e.g. 0V and 5V), transition times between the two levels (i.e. rise time, fall time), and a period that is related to the pulse width. The shorter the period and faster the transition times, the higher the data rate and the frequency of the signal. The interface system commonly provides the necessary signal modifications to the electrical characteristics of the output signal to match the input requirements of the receiver. For example, the maximum input voltage for a certain receiver may be lower than the voltage of the signal of a corresponding output device.

Hence, the interface system must attenuate the signal prior to reaching the input terminals of the receiver.

[0003] Another common interface mismatch is the DC voltage component of the signal, commonly referred to as the DC offset. For example, a signal traveling through a coaxial cable is typically an AC signal referenced to the static ground or DC voltage level of the outer conductor of the coaxial cable. However, a receiver may require an input signal with a certain DC offset to provide a DC bias voltage and prevent saturation of its input state. Therefore, to overcome DC offset mismatch problems, AC or capacitive coupling interface systems are desired over direct or DC coupling systems.

[0004] Some AC coupling interface systems employ a resistive-capacitive network (RC) to couple fixed impedance output devices with receivers. The capacitive and resistive elements of the network are chosen to transmit the signal without distorting the information carried by the signal. In addition, selection of the elements should take into account the modifications to the electrical characteristics of the signal required to match the receiver input requirements. The product of the resistance times the capacitance of the RC network elements provides the RC time constant (TC) that must be selected in relation to the period of the data signal to avoid signal distortion.

[0005] Another factor to consider in the design of AC coupling interface systems is the energy transfer between the output device and the receiver. In order to transfer the maximum signal energy through the interface system from the output device to the receiver, the interface system should provide proper impedance matching between the characteristic output impedance of the output device and input impedance of the receiver. For example, in an RC network interface system, the resistive element is chosen to match the characteristic impedance of the

output device, e.g. a transmission line, a GBIC, or the like. Proper impedance matching, or termination prevents signal reflections at the interface that may cause distortions (i.e. ringing). Hence, to provide proper matching to a fixed impedance device, the resistive elements of an RC network may be predetermined by the characteristic impedance of the output device. Similarly, the capacitive elements may be determined by the period of the signal, as described above, the capacitive value must be selected to provide a TC that does not cause signal distortion.

[0006] A problem arises when the data signals supplied to the receiver recur at data rates that are orders of magnitude apart, the characteristic output impedance of the output device is very low (tens to hundreds of ohms), and the receiver is configured to receive multiple standard digital data rates. For example, a high-speed signal output from an optical GBIC terminal at 2.5 Gbps and a lower-speed RS 232 signal at 9.6 Kbps may be supplied at different times to the input of a wide-band receiver through the same low impedance transmission line. In this situation, an AC coupling interface system must provide matching for the low impedance of the output device while preserving the signal data integrity, i.e. not distorting the signal. Such an interface system including an RC network and operating the very low characteristic output impedance (e.g. 50 to 100 ohms) would require an impractical, prohibitively high value capacitive element to maintain a reasonable RC time constant that does not distort the lower frequency signal beyond practical use.

SUMMARY OF THE INVENTION

[0007] In accordance with an illustrated embodiment of the present invention, an interface system is provided that enables digital data signals of different data rates to be transmitted at different times from a low impedance node to a broadband, wide-spectrum receiver through a

dynamic load. The interface system allows transmission of low data rate signals and high data rate signals with minimal resultant signal distortion using capacitive elements of practical size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a high level block diagram of a system incorporating an interface system according to the present invention;

[0009] Figure 2A is a schematic diagram of one embodiment of a circuit for implementing an AC coupling system according to the present invention;

[0010] Figure 2B is a schematic diagram of one embodiment of a circuit for implementing an AC coupling system according to the present invention

[0011] Figure 3 is a schematic diagram of an alternative embodiment of a double-ended AC coupling system according to the present invention.

[0012] Figure 4 is a circuit schematic of one embodiment of the present invention for operation on differential applied signals.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Referring now to Figure 1, there is shown a block diagram of a system incorporating an interface system 140 according to the present invention. Two data networks, a high data rate network 100 and a low data rate network 105 are shown. In one embodiment, high data rate network 100 may be a Gigabit Ethernet network. Alternatively, high data rate network 100 may be a SONET/SDH fiber network, or some other fiber-optic network operating at high data rates (e.g. 531 Mbps, 1062 Mbps, 2.5 Gbps, or the like). It should be noted that the present invention may operate with other high data rate networks (e.g. in the Megabit to multiple Gigabit

per second range) now existing or as may be developed in the future. Similarly, the low data rate network 105 may be any data network communicating according to one of several network protocols or standards that use a data rate or frequency that is orders of magnitude smaller than the high data rate network (e.g. in the Kilobit-per-second range). For example, the low data rate network 105 may transmit data at approximately 9.6 Kbps according to an EIA/TIA RS-232 protocol, or a CCITT data protocol (e.g. X.21, V.24).

[0014] High data rate network 100 supplies high data rate signals to high speed data system 110 and low data rate network 105 supplies low data rate signals to low speed data system 115 each at their respective operating data rate. High-speed data system 110 receives high data rate data signals from the high data rate network 100 and after some processing supplies high data rate signal 120 to node 130. Low-speed data system 115 receives low data rate data signals from the low data rate network 105 and after some processing supplies low data rate signal 120 to node 130. In one embodiment, high data rate signal 120 and low data rate signal 125 may be digital signals in the form of a square waves encoding data using a pulse or pulse width modulation scheme, however, other wave forms and modulation schemes may be used (e.g. amplitude modulation, phase shift keying, quadrature phase shift keying, and the like).

[0015] Similarly, in one embodiment, high-speed data system 110 may be a terminal device, such as, a GBIC Terminal for optical data communications, a high speed multiplexer, a demultiplexer, a high speed SERDES, or the like. In an alternative embodiment, high-speed data system 110 may be a fixed impedance transmission line (e.g. 50-ohm or 75-ohm coaxial cable, twisted pair cable, stripline, microstripline, a printed circuit board (PCB) controlled impedance trace, or the like). Likewise, in one embodiment, low-speed data system 115 may be a terminal device, such as data communication equipment (DCE) (e.g. a data modem), or may be a fixed

impedance transmission line. The physical conductors of the data signals, high data rate data signal 120 and low data rate data signal 125, are merged at a node 130. Node 130 may be any device capable of merging the paths of data signals of different data rates that are supplied to the node 130 at different times, for example, a two-input-one-output cable connector, or a multiplexer, or a SERDES, or a hub, or the like. It should be noted that there are many other devices capable of merging the paths of data signals of different data rates that could be used in alternative embodiments of the present invention. Further, in one embodiment of the present invention, data systems 110 and 115 and node 130 may all be combined into one device or system. For example, in one embodiment, high data rate network 100 and low data rate network 105 may share the same physical infrastructure and data systems 110 and 115 are part of that shared infrastructure. Then, node 130 may be a fixed impedance transmission line (e.g., 50-ohm or 75-ohm coaxial cable, twisted pair cable, stripline, microstripline, a printed circuit board (PCB) controlled impedance trace, or the like) carrying both data signals 120 and 125 supplied at different times to interface system 140. It should be noted that node 130 supplies the signals of different data rates to the interface system 140 at different times, i.e. high data rate signal 120 is not combined with low data rate signal 125 because they only travel through the connection between node 130 and interface system 140 at different times.

[0016] Data signals 120 and 125 supplied to node 130 become the corresponding input signals 121 and 126 supplied to receiver 150 after undergoing modifications through interface system 140. Interface system 140 connects the output of the node 130 to the receiver 150 and modifies electrical characteristics of the signals to convert data signals 120 and 125 into corresponding data signals 121 and 126 while preserving the data. Data signals 121 and 126 carry the same data as signals 120 and 125 but are compatible with the input requirements of

receiver 150. The modifications of electrical characteristics may include, without limitation, alter DC offset voltage, limit maximum peak voltage, or change current. For example, in one embodiment of the present invention, interface system 140 may provide AC coupling to change the DC offset of the data signals from a 0V ground level to a certain DC bias voltage required for the proper operation of an input state of receiver 150.

[0017] Interface system 140 has an input terminal 141 that receives at different times the data signals 120 and 125 from node 130. The input terminal is connected to a high data rate module 143 and a low data rate module 144. High data rate signal 120 appearing at the input terminal 141 is transmitted through the high data rate module 143 which performs the necessary electrical characteristic modifications to meet the input requirements of receiver 150. High data rate module 143 is configured to process the high data rate signal 120 into high data rate signal 121 without losing data integrity, i.e. without distorting the high data rate signal 120 beyond usability. Similarly, low data rate signal 125 appearing at the input terminal 141 is transmitted through the low data rate module 144 which performs the necessary electrical characteristic modifications to meet the input requirements of receiver 150. Low data rate module 144 is configured to process the low data rate signal 125 into low data rate signal 126 without losing data integrity, i.e. without distorting the low data rate signal 125 beyond usability. High data rate module 143 and low data rate module 144 are connected to the output terminal 142 of the interface system 140 to transmit the modified data signals 121 and 126 to the receiver 150. In one embodiment of the present invention, the high data rate module 143 and low data rate module 144 may be combined into a single dual function module such as, for example, an RC network. In alternative embodiments, receiver 150 may be a wide-band receiver, a high-speed post amplifier, a differential amplifier, or the like. For example, receiver 150 may be an

SY88993AV (available from Micrel, Inc. of San Jose, California) with an input frequency range of approximately 0 to 2.5 GHz.

[0018] Further, the system illustrated in Figure 1 may comprise more than two data networks. For clarity of explanation, embodiments with only two data signals from two data networks are described. However, it should be noted that the same principles apply to a third, fourth, and multiple numbers of data signals, each with a different data rate.

[0019] Now referring to Figures 2A and 2B, two embodiments of the interface system 140 are shown at the circuit level. Node 130 is represented in the embodiment shown in Figures 2A and 2B as a grounded, single ended, output device such as, for example, a fixed impedance transmission-line (e.g. a 50 or 75 ohm coaxial cable, or a 100-ohm twisted pair cable, or the like). Interface system 140 is represented by two different embodiments of similar functionality but slightly different arrangement of elements, RC network interface systems 240a and 240b. RC network interfaces 240a and 240b receive data signals 120 and 125 from node 130, modify the electrical characteristics of data signals 120 and 125, and supplies to the receiver input 231 corresponding data signals 121 and 126 that meet the input requirements of receiver 230. In one embodiment shown in Figure 2A, RC network interface system 240a is an AC coupling interface system including an RC network in a high-pass configuration. Capacitive element 250 connects the node 130 to receiver input 231 of receiver amplifier 230 and to one node of the parallel combination of resistive element 255 and the series combination of resistive element 245 and capacitive element 235. The other node of parallel combination of resistive element 255 and the series combination of resistive element 245 and capacitive element 235 is connected to AC ground 260 and to the other input 232 of receiver amplifier 230. In one embodiment, AC ground 260 may be a DC bias network that provides a biasing DC voltage at the input of receiver

amplifier 230 at a level centered within the input common mode range of the input stage of amplifier 230. AC ground 260 thus provides the necessary DC offset to the input of receiver amplifier 230 following the capacitive decoupling of the DC component of the applied signals.

[0020] The product of the component values of the capacitive element 235 and resistive element 245 determine a fast RC time constant (TC) of the RC network interface system 240a. Similarly, capacitive element 250 and resistive element 255 determine a long RC time constant of the RC network interface system 240a. As described above, the principles of the invention can be extended for operation with more than two different signal data rates. Accordingly, in other embodiments other time constants may be required for the operation of the RC network interface system 240a with more data signals at different data rates. To provide the necessary time constants, series combinations of resistive and capacitive elements (similar to the connection of elements 245 and 235) can be connected in parallel with resistive element 255 as additional branches.

[0021] The short time constant, which is determined by capacitive element 235 and resistive element 245, controls the response of the RC network interface system 240a to the rising and falling edges of the square wave form of the high data rate signal 120. The rising and falling edges of the square wave data signals comprise dominant high frequency components. A resistive element 245 that establishes the fast RC time constant is selected to closely match the fixed impedance of the node 130 (e.g. 50 or 75 ohm transmission line, microstripline, 100 ohm twisted pair, or the like) and the capacitance of capacitive element 235 is selected to permit charging approximately as fast as the rise time of the square wave form of the high data rate signal. Similarly, the long time constant determined by capacitive element 250 and resistive element 255 controls the response of the RC network interface system 240a on applied signals of

low data rates. Low data rate signals are more dominantly characterized by a longer pulse width or period than the pulse width or period of high data rate signals. In order to avoid distortion of the data in applied low data rate signals, the capacitance of capacitive element 250 is selected to hold the charge from the applied data signals for a period longer than the period of the applied low data rate signals. In addition, the resistance value of resistive element 255 is selected to provide a discharge path for capacitive element 250 over a time-constant interval longer than the width or period of an applied low data rate signal, thereby providing the long TC for RC network interface system 240a.

[0022] The selection of the elements in the RC network interface system 240a may be guided by the following relationships. The value of resistive element 255 should be selected to be much higher resistance than the value of the resistive element 245 and therefore form a much longer, slower, or larger time constant with capacitive element 250 than the shorter, faster, or smaller time constant determined by capacitive element 235 and the lower-value resistive element 245. In addition, capacitive element 250 is selected to have much higher capacitance than capacitive element 235. Hence, capacitive element 235 discharges a significant percentage of its charge through the lower-value resistive element 245 long before the higher-value capacitive element 250 loses a significant percentage of its greater charge. The RC network interface system 240a thus behaves as a dynamic AC load. Specifically, the AC load is the low impedance termination of the resistive element 245 (that matches the fixed impedance of the node 130) for high data rate signals, and the AC load is the high impedance provided by resistive element 255 and capacitive element 250 for low data rate signals. It should be noted that the AC ground 260 may be a biasing network that sets the proper DC bias voltage in combination with resistive element 255 for the receiver amplifier 230.

[0023] In one embodiment of the present invention, the capacitive element 235 is about 0.1uF and resistive element 245 is about 50 ohms. Similarly, capacitive element 250 is about 5uF and resistive element 255 is about 50 K-ohms. In this exemplary embodiment, capacitive element 250 has 50 times more capacitance than capacitive element 235, and the resistance of resistive element 255 is three orders of magnitude larger than resistive element 245. These values provide a short TC of 5 microseconds and a long TC of 250 milliseconds for operation on a low data rate signal having a period that may be approximately 50000 times longer than the period of a high data rate signal to provide an effective AC coupling interface system for a 50-ohm transmission line carrying 2.5Gbp and 9.6Kbps data signals to a wide band receiver 230.

[0024] Now referring to Figure 2B, another embodiment of the present invention is shown in which RC network interface system 240b has a different arrangement of elements as compared to RC network interface system 240a. However, RC network interface system 240a and 240b are functionally equivalent and the same operating principles described above with reference to Figure 2A apply to the RC network interface system 240b shown in Figure 2B. Capacitive element 250 is connected to supply input data signals 121 and 126 to one input terminal 231 of receiver amplifier 230 and to resistive element 345, which is connected to one node of the parallel combination of capacitive element 235 and resistive element 355. The parallel combination is connected to AC ground 260 and to the other input 232 of receiver amplifier 230.

[0025] In this embodiment resistive element 355 has a much larger resistance value than resistive element 345, and capacitive element 250 has larger capacitance than capacitive element 235. The long TC is the product of capacitive element 250 and the sum of resistive elements 345 and 355.

[0026] Figure 3 shows an alternative embodiment of the present invention of a differential interface system 440 including an RC network in a differential circuit topology. Signals 420+/420- and 425+/425- are differential data signals that define the data in the difference between the two signals. Differential signal 420+/420- is high data-rate signal and differential signal 425+/425- is a low data-rate signal. Advantages of using differential circuit topologies include, without limitation, robustness against common mode noise and crosstalk, faster data transfer, reduced electromagnetic interference (EMI), and thermal drift. Differential signals 420+/420- and 425+/425- are transmitted from nodes 400a and 400b to differential amplifier 430 through the differential interface system 440. In one embodiment, node 400a is a fixed impedance transmission line carrying one side of the two differential signals, i.e., the positive polarity side, 420+ and 425+, and node 400b is a second fixed impedance transmission line carrying the other side of the two differential signals, i.e., the negative polarity side, 420- and 425-.

[0027] Differential interface system 440 converts applied signals 420+/420- and 425+/425- into output signals 421+/421- and 426+/426- that are compatible with the input requirements for differential amplifier 430. Elements 450a, 445a, 455a, and 435a are a differential half-circuit that provides the AC coupling described above with reference to Figure 2A for one side of the differential signals (i.e., the positive polarity sides, 420+ and 425+), and elements 450b, 445b, 455b, and 435b are the other differential half-circuit that provides similar AC coupling for the opposite side of the differential signal (i.e., the negative polarity sides, 420- and 425-). In this embodiment, AC ground 460, in addition to the DC bias voltage described above also provides correction for any DC offset mismatch between the two branches of the differential signal that may occur upon conversion from a single-ended to a double-ended differential signal.

[0028] Now referring to Figure 4, there is shown a schematic diagram of a differential circuit topology according to the principles of the present invention. The embodiment shown in Figure 4 is particularly optimized for operation with data signals at about 9.6 Kbps and 2.5 Gbps data rates, with square waves having about 80 pico-second through 100 nano-second transition times. Transmission lines 500a and 500b are connected to the differential RC network interface system 520 that AC couples the applied data signals to differential amplifier stage 530. Transmission lines 500a and 500b are referenced to ground 210. Differential amplifier stage 530 includes two transistors 532a and 532b biased by collector resistors 531a and 531b and current source 533. To maintain the inputs to transistors 532a and 532b within the common mode range, voltage source 560 provides a reference of about 1.3 Volt DC bias voltage and also provides an AC ground for the data signals.

[0029] In this embodiment, capacitors 550a and 550b are connected to apply the input differential data signals from the transmission lines 500a and 500b to the nodes formed as the common connections of the bases of transistors 532a and 532b, the resistors 565a and 565b, and the resistors 545a and 545b that are each connected in series with capacitors 535a and 535b. Resistors 565a and 565b have a resistance of about 50 K-ohm and resistors 545a and 545b have a resistance of about 50 ohm. Capacitors 550a and 550b have a capacitance of about 5uF and capacitors 535a and 535b have a capacitance of about 100nF and are connected to the reference node of voltage source 560 and to resistors 565a and 565b. Voltage source 560 supplies the system bias voltage 570 (Vcc). In this embodiment, the combinations of capacitors 535a and 535b with resistors 545a and 545b determine the short time constants for each branch of the differential signals. These time constants control the response of the interface system 520 to the 2.5 Gbps data signals with the associated square wave transitions. Similarly, the long time

constants for each branch of the differential signals are determined by the combination of capacitors 550a and 550b with the large-value resistors 565a and 565b. These time constants control the response of interface system 530 to the 9.6 Kbps data signals with longer periods between square wave transitions.

[0030] Therefore, in the embodiment shown in Figure 4, the 2.5 Gbps differential signal is applied across the 50-ohm load of resistors 545a and 545b and charges capacitors 535a and 535b. For the 9.6 Kbps differential signal, an applied data signal pulse charges capacitors 550a and 550b that are slowly discharged through the 50 K-ohm resistors 565a and 565b. Thus, in the embodiment of Figure 4, the interface system couples transmission lines 500a and 500b to differential amplifier stage 530 for 2.5 Gbps and 9.6 Kbps signals without significant distortion of the usable data signal waveforms.